ECEN 204 Electronic Design **Test 4**

Due 1659 hrs on 22 October 2020.

Name: ……

Student Number:…….

Instructions

Attempt all questions Total = 80 marks

The test will be available on ECS Wiki after 1200 hrs (NZ time) on Wednesday 21 October. You will have at least 24 hours available to complete and hand in.

Please upload you answer scripts on **ECS Wiki submission system**. The submission system **closes at 1659hrs (NZ time) on the 22nd October**.

Type or neatly write your answers in the spaces provided. You can also electronically draw your sketches on the document or else draw in another package and then import into this document. Show the details of your workings where appropriate – do not just show final answer.

The test should be completed **individually**, that is you may not consult with anyone to obtain answers but is "open book" – you may consult your class notes/videos or even the internet.

Save your document with a filename "your surname"_"your initials"_ ECEN204_Test4 and ensure that you submit this in the ECS Wiki submission system no later than 459 pm (NZ time) on Thursday 22 October 2020. Please submit as good quality pdf or Word document.

All these questions deal with n-type enhancement MOSFETs. Remember, such a MOSFET will be in saturation mode if: $V_{GS} > V_t$ and $V_{GD} < V_t$. If the MOSFET is in the saturation region then:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)^2 \quad \text{and} \quad i_d = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)v_{gs}$$

The transconductance is defined by:

$$g_m = \frac{i_d}{v_{gs}} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)$$

Question 1 [20]

Design the circuit shown in Fig. 1 (i.e. find values for the resistors R_D and R_S) so that the transistor operates with I_D = 0.4 mA and V_D = +1 V. Assume that V_t = 2 V, $\mu_n C_{ox}$ = 20 μA/V^2, L = 10 μm and W = 400 μm.

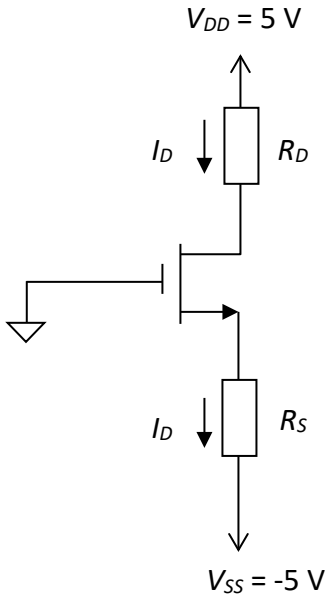
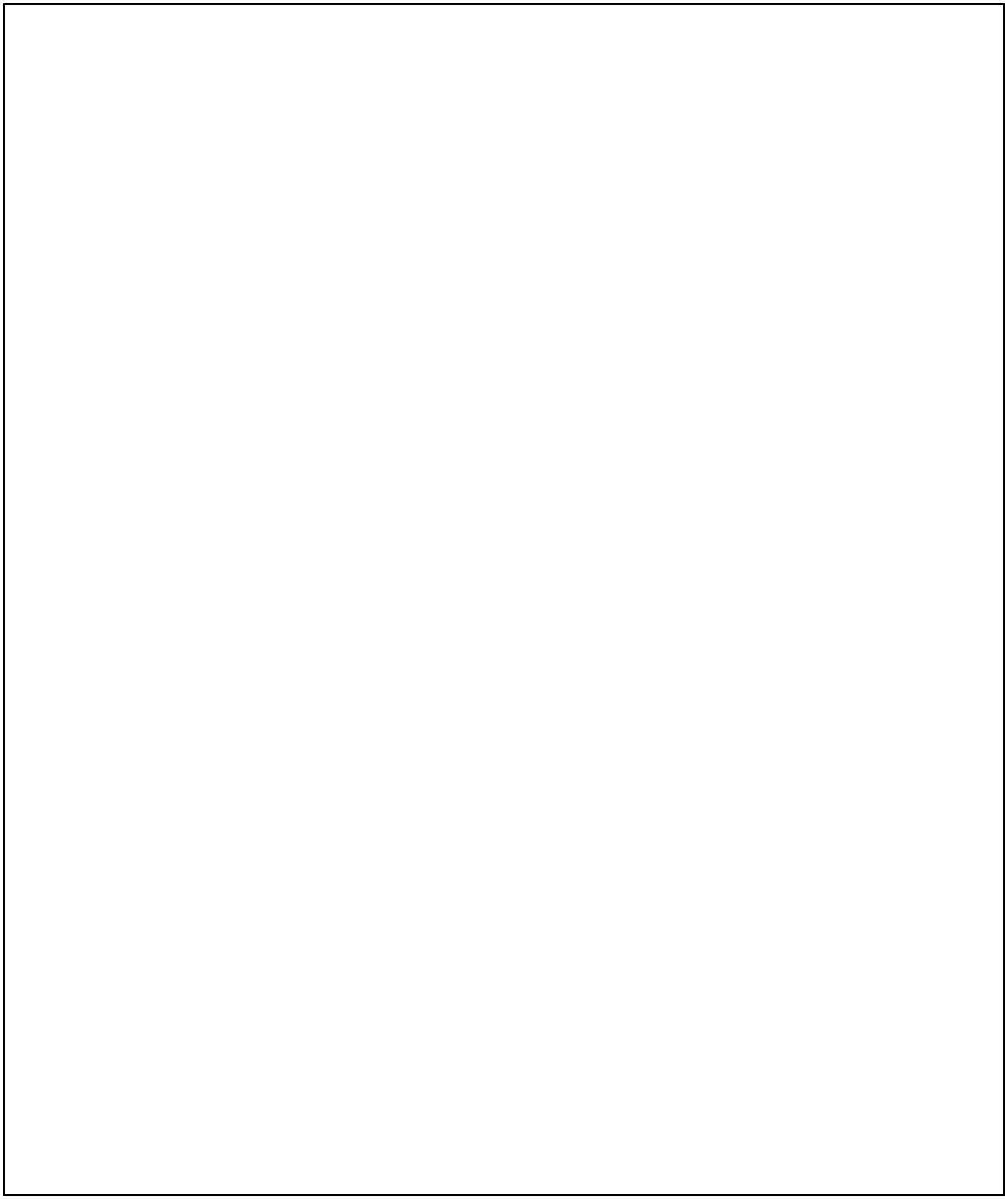


Fig. 1



Question 2 [20]

Design the circuit in Fig. 2 to obtain a current I_D of 0.4 mA. Find the value required for *R* and find the dc voltage V_D. Assume the values for V_t, $\mu_n C_{ox}$, *L* and *W* as in Q1.

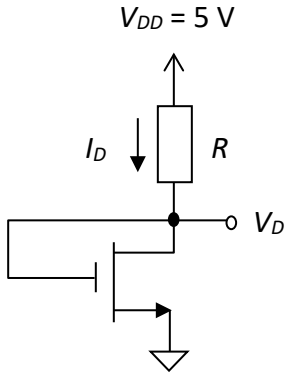


Fig. 2

Question 3 [20]

For the circuit shown in Fig. 3 determine if the MOSFET is in saturation mode and find the drain current. The transistor has

V_t = 2 V and $\mu_n C_{ox} W/L$ = 2 mA/V^2.

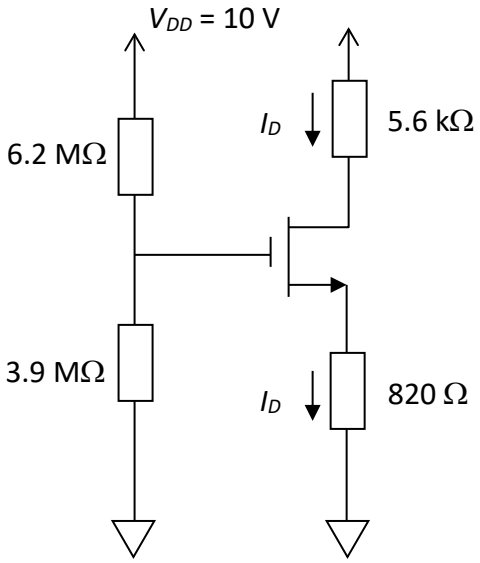


Fig. 3

Question 4 [20]

For the circuit shown in Fig. 4:

(a) find the dc quantities I_D and V_D;

(b) calculate the value of g_m at this bias point;

(c) calculate the value of the voltage gain.

Assume V_t = 2 V, $\mu_n C_{ox} W/L$ = 1 mA/V^2 and V_{GS} = 4 V.

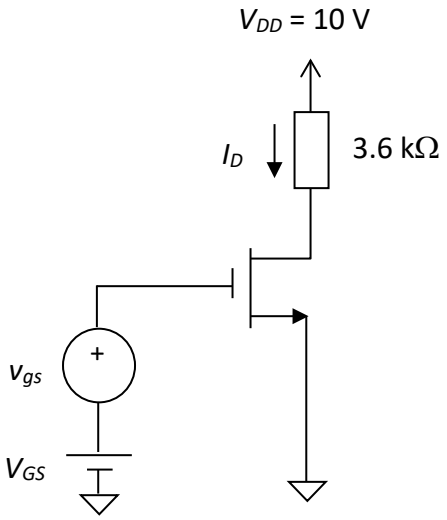


Fig. 4

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ECEN 204 **Assignment 5**

Total marks: 40

Below are the problems for this assignment. Do your calculation as needed and then put your final answers as well any discussion or plots in the spaces required. Submit this document with a filename:

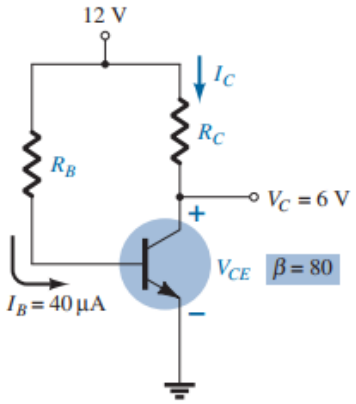
ECEN204_Assmt5_2021_"your surname"-"your initial" on the Wiki submission system no later than Monday 4 October by 11.59 pm.

Name: ……..

Student Number:…….

Q1. Given the following figure, determine:

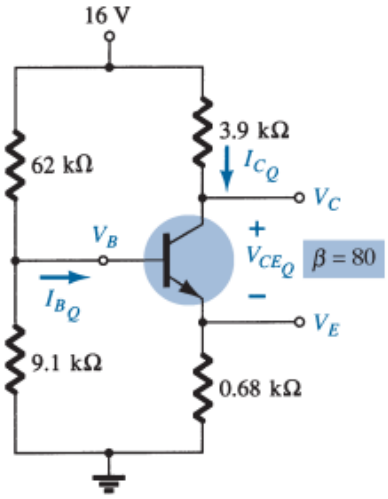
a) I_C
b) R_C
c) R_B
d) V_{CE}.



Answer (10)

Q2. For the following voltage divider biased amplifier circuit, find:

a) I_{BQ}
b) I_{CQ}
c) V_{CEQ}
d) V_C
e) V_E
f) V_B.



Answer (15)

Q3. Design a voltage-divider bias network using a supply of 24 V, a transistor with a beta of 110, and an operating point of I_{CQ} = 4 mA and V_{CEQ} = 8 V. Choose $V_E = 1/8V_{CC}$. Use standard values.

Answer: (15)

EEEN 204 **Assignment 5**

Total marks: 55

Below are the problems for this assignment. Do your calculation as needed and then put your final answers as well any discussion or plots in the spaces required. Submit this document with a filename:

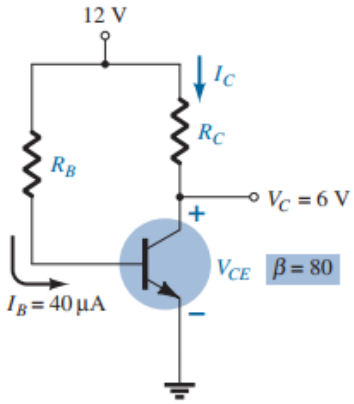
EEEN204_Assmt5_2022_"your surname"-"your initial" on the Wiki submission system no later than Friday 14 October by 11.59 pm.

Name: ……..

Student Number:…….

Q1. Given the following figure, determine:

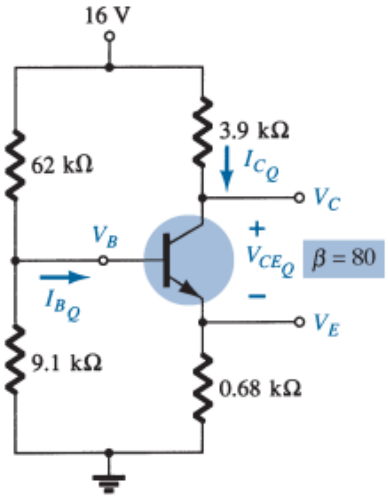
a) I_C
b) R_C
c) R_B
d) V_{CE}.



Answer (10)

Q2. For the following voltage divider biased amplifier circuit, find:

a) I_{BQ}
b) I_{CQ}
c) V_{CEQ}
d) V_C
e) V_E
f) V_B.



Answer (15)

Q3. Design a voltage-divider bias network using a supply of 24 V, a transistor with a beta of 110, and an operating point of I_{CQ} = 4 mA and V_{CEQ} = 8 V. Choose V_E = 1/8V_{CC}. Use standard values and select the components available in the market. Do the second iteration with the market components and compare the results.

Answer: (15 + 15 marks for component selection and second iteration of design)

Name: _____

EEEN 204 Electronic Devices

Test 2: 3 November 2023

There are **50 marks** worth of questions in this test. You are to answer all questions and you have **60 minutes** in which to do so. This test is not open book but you are allowed two sides A4 of hand written notes. If you need additional space then feel free to write on the back of the pages. ***Good luck, have fun.***

Unless otherwise stated, you should assume V_{DD} = 5.0 V and that

For nMOS devices V_t = 1.0 V V_{td} = -3.0 V

For pMOS devices V_{tp} = -1.0 V V_{tpd} = 3.0 V

For FETS in saturation, $I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2$

In non-saturation $I_{DS} = \beta\left((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right)$

(1) Draw the schematic diagram of a pMOS inverter that uses one pMOS enhancement mode and one pMOS depletion mode transistor.

[3 marks]

(2) Derive an expression for the steady state **output current** of the inverter gate designed in (1) above, if its output was connected to an identical inverter.

[2 marks]

(3) What **two** conditions are required for a **pMOS depletion** mode transistor to be operating in its **saturated** mode?

[3 marks]

(4) Name **two** elements that could be added as extrinsic impurities to silicon in order to make it **p-type**?

[2 marks]

(5) Draw the block diagram for a CMOS transistor clearly illustrating all the layers.

[2 marks]

(6) Calculate the voltage swing of a standard nMOS inverter (one enhancement mode and one depletion mode transistor) where the pull-up (depletion transistor) has a L:W ratio of **8:1**, and the pull-down (enhancement mode transistor) has a L:W ratio of **1:1**. This is an 8:1 inverter. You may assume that $V_{in(low)}$ is < V_t, and $V_{in(high)}$ is V_{DD}.

[5 marks]

(7) What **2 conditions** are required for an npn bipolar transistor to be operating in its **saturation** mode? Express your answer in terms of V_{BE}, V_{CB}. It is not acceptable to just state "forward" or "reverse" bias.

[2 marks]

(8) Would a bipolar or a MOSFET transistor be more radiation **immune**? *Briefly* explain your answer.

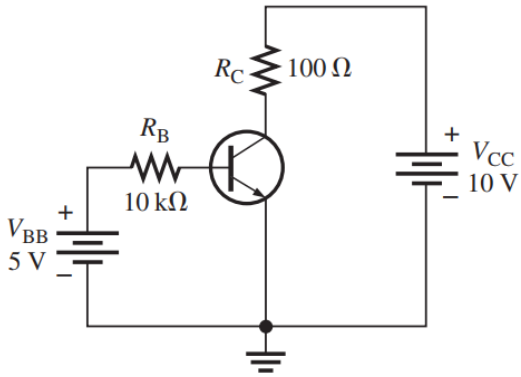
[3 marks]

(9) Determine α and β for a BJT given an emitter current of 5.602 mA and a base current of 50 μA.

[3 marks]

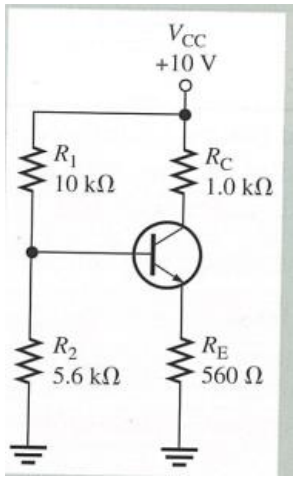
(10) Determine I_B, I_C, I_E, V_{CE} and V_{CB} for the circuit on the right if $\beta_{DC} = 50$.

[7 marks]



(11) Determine V_{CE} and I_C in the stiff voltage-divider based circuit on the right if $\beta_{DC} = 50$.

[8 marks]



(12) For the circuit on the right, determine if the nMOSFET is in saturation mode and find the drain current I_D. The transistor has a threshold voltage $V_t = 2$ V and $\beta = 2$ mA/V^2.

[10 marks]